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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,814	10/26/2001	Michael S. Foster	030048036US	9498

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EXAMINER

BENGZON, GREG C

ART UNIT	PAPER NUMBER
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2144

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/039,814

Applicant(s)

FOSTER ET AL

Examiner

Greg Bengzon

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 April 2002 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

This application has been examined. Claims 1-41 are pending.

Priority

This application claims benefits of priority from US Provisional Application 60/287069 filed April 27, 2001.

The effective date of the subject matter in the claims in this application is April 27, 2001.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 02/19/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 18, 26, 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 recites the limitation "computer system of Claim 1". There is insufficient antecedent basis for this limitation in the claim.

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Claims 26 and 41 contains the trademark/trade name 'InfiniBand'. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe [3] and, accordingly, the identification/description is indefinite.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata (US Patent 6108708).

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With respect to Claim 1, Iwata discloses a method in a computer system for reconfiguring a path between a source node and a destination node, the method comprising: (Figures 1-4, Figure 6-10, Column 7 Lines 1-35, Column 8 Lines 1-15) establishing a first path between the source node and the destination node, the path having a virtual address; (Column 1 Lines 45-65) providing the virtual address to the source node for use in transmitting data from the source node to the destination node via the established path; (Column 6 Lines 50-55, Column 8 Lines 50-65) and after providing the virtual address to the source node, establishing a second path between the source node and the destination node so that when the source node transmits data using the provided virtual address the data is transmitted via the second path rather than via the first path. (Column 9 Lines 1-5, Lines 40-65, Column 10 Lines 30-40, Column 12 Lines 35-45)

With respect to Claim 2, Iwata discloses the method of claim 1 wherein the establishing of the second path is performed transparently to the source node. (Column 6 Lines 55-65, Column 9 Lines 1-5, Lines 40-65, Column 12 Lines 35-45)

With respect to Claim 3, Iwata discloses the method of claim 1 wherein the path is established through a network of switches. (Column 1 Lines 45-65, Column 6 Lines 30-40)

With respect to Claim 4, Iwata discloses method of claim 1 wherein the path is established through switches with ports and wherein the establishing of a path includes identifying a source-side port and a destination-side port for each switch. (Column 6 Lines 20-50, Column 8 Lines 1-15)

With respect to Claim 5, Iwata discloses the method of claim 4 wherein the establishing of the path includes providing the virtual address to each source-side port of a switch in the path. (Column 8 Lines 1-15, Column 12 Lines 1-15)

With respect to Claim 6, Iwata discloses the method of claim 5 wherein the virtual address of source-side port is used to map the source-side port to the destination-side port of the switch. (Column 10 Lines 30-65)

With respect to Claim 7, Iwata discloses the method of claim 1 including identifying a virtual address for sending data from the source node to the destination node, the identified virtual address being provided to the source node. (Column 6 Lines 50-55, Column 8 Lines 50-65)

With respect to Claim 8, Iwata discloses the method of claim 7 wherein the identified virtual address is not currently used by any source-side ports of the switches.

(Column 6 Lines 55-65, Column 12 Lines 1-5)

With respect to Claim 9, Iwata discloses the method of claim 7 wherein each port of each switch has a virtual address table for mapping virtual addresses to another port of the switch. (Column 10 Lines 30-65)

With respect to Claim 10, Iwata discloses the method of claim 1 wherein when data is received at a port of a switch, the virtual address of the data is used to retrieve an indication of another port and the data is sent out of the switch through the other port. (Column 10 Lines 30-65)

With respect to Claim 11, Iwata discloses the method of claim 1 wherein the establishing of path from the source node to the destination node includes identifying a source-side port and a destination-side port of each switch in the path. (Column 10 Lines 30-65)

With respect to Claim 12, Iwata discloses the method of claim 1 wherein the data is a Fibre Channel frame. (Column 1 Lines 1-25) The Examiner notes that the Fibre Channel protocol was designed to operate on ATM networks.

With respect to Claim 13, Iwata discloses the method of claim 1 wherein the switches are Fibre Channel compatible. (Column 1 Lines 1-25) The Examiner notes that the Fibre Channel protocol was designed to operate on ATM networks.

With respect to Claim 14, Iwata discloses the method of claim 1 wherein the switches are interconnect fabric modules. (Column 1 Lines 45-55)

With respect to Claim 15, Iwata discloses a computer system for reconfiguring a path between a source node and destination nodes, (Figures 1-4, Figure 6-10, Column 7 Lines 1-35, Column 8 Lines 1-15) comprising: a component that establishes a first path between the source node and a first destination node, the path having a virtual address, (Column 1 Lines 45-65) the first path being identified by a virtual address, so that when the source node transmits data using the virtual address, the data is transmitted via the first path; and a component that, after establishing the first path, (Column 6 Lines 50-55, Column 8 Lines 50-65) establishes a second path between the source node and a second destination node, the second path being identified by the virtual address so that when the source node transmits data using the provided virtual address after the second path is established, the data is transmitted via the second path. (Column 9 Lines 1-5, Lines 40-65, Column 10 Lines 30-40)

With respect to Claim 16, Iwata discloses the computer system of claim 15 including: a component that provides the virtual address to a source node for use in transmitting data via the first path before the second path is established and via the second path after the second path is established. (Column 6 Lines 55-65, Column 8 Lines 50-65, Column 12 Lines 35-45)

With respect to Claim 17, Iwata discloses the computer system of claim 15 wherein the establishing of the second path is performed transparently to the source node. (Column 6 Lines 55-65, Column 9 Lines 1-5, Lines 40-65, Column 12 Lines 35-45)

With respect to Claim 18, Iwata discloses the computer system of claim 1 wherein the path is established through a network of switches. (Column 1 Lines 45-65, Column 6 Lines 30-40)

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With respect to Claim 19, Iwata discloses the computer system of claim 15 wherein the paths are established through switches with ports and wherein the establishing of a path includes identifying a source-side port and a destination-side port for each switch in the path. (Column 6 Lines 20-50, Column 8 Lines 1-15)

With respect to Claim 20, Iwata discloses the computer system of claim 19 wherein the virtual address is used by source-side ports to map the source-side port to the destination-side port of the switch. (Column 10 Lines 30-65)

With respect to Claim 21, Iwata discloses the computer system of claim 15 including: a component that identifies a virtual address for sending data from the source node to a destination node, the identified virtual address being provided to the source node. (Column 6 Lines 50-55, Column 8 Lines 50-65)

With respect to Claim 22, Iwata discloses the computer system of claim 21 wherein the identified virtual address is not currently used by any source-side ports of the switches. (Column 6 Lines 55-65, Column 12 Lines 1-5)

With respect to Claim 23, Iwata discloses the computer system of claim 21 wherein each port of each switch has a virtual address table for mapping virtual addresses to another port of the switch. (Column 10 Lines 30-65)

With respect to Claim 24, Iwata discloses the computer system of claim 15 wherein when data is received at a port of a switch, the virtual address of the data is used to retrieve an indication of another port and the data is sent out of the switch through the other port. (Column 10 Lines 30-65, Column 11 Lines 1-35)

With respect to Claim 25, Iwata discloses the computer system of claim 15 wherein the data is a Fibre Channel frame. (Column 1 Lines 1-25) The Examiner notes that the Fibre Channel protocol was designed to operate on ATM networks.

With respect to Claim 26, Iwata discloses the computer system of claim 15 wherein the data is an InfiniBand frame. (Column 1 Lines 1-25) The Examiner notes that the Fibre Channel protocol was designed to operate on ATM networks.

With respect to Claim 27, Iwata discloses the computer system of claim 15 wherein the first destination node and the second destination node are different nodes. (Column 6 Lines 25)

With respect to Claim 28, Iwata discloses the computer system of claim 15 wherein the first destination node and the second destination node are the same node. (Column 6 Lines 25)

With respect to Claim 29, Iwata discloses a computer system for reconfiguring a path between a source node and a destination node, (Figures 1-4, Figure 6-10, Column 7 Lines 1-35, Column 8 Lines 1-15) comprising: means for establishing a first path between the source node and the destination node, the path having a virtual address; (Column 1 Lines 45-65) and means for establishing a second path between the source node and the destination node (Column 6 Lines 50-55, Column 8 Lines 50-65) so that data transmitted using the virtual address is routed via the first path before the second path is established and via the second path after the second path is established. (Column 9 Lines 1-5, Lines 40-65, Column 10 Lines 30-40)

With respect to Claim 30, Iwata discloses the computer system of claim 29 including: means for providing the virtual address to the source node for use in transmitting data to the destination node. (Column 6 Lines 45-55)

With respect to Claim 31, Iwata discloses the computer system of claim 29 wherein the establishing of the second path is performed transparently to the source node. (Column 6 Lines 55-65, Column 9 Lines 1-5, Lines 40-65, Column 12 Lines 35-45)

With respect to Claim 32, Iwata discloses the computer system of claim 29 wherein the path is established through a network of switches. (Column 6 Lines 20-35)

With respect to Claim 33, Iwata discloses the computer system of claim 32 wherein the paths are established through switches with ports and wherein the means for establishing of a path includes identifying a source-side port and a destination-side port for each switch in the path. (Column 6 Lines 20-50, Column 8 Lines 1-15)

With respect to Claim 34, Iwata discloses the computer system of claim 33 wherein the virtual address is used by source-side ports to map the source-side port to the destination-side port of the switch. (Column 10 Lines 30-65)

With respect to Claim 35, Iwata discloses the computer system of claim 32 wherein the switches are interconnect fabric modules. (Column 1 Lines 45-55)

With respect to Claim 36, Iwata discloses the computer system of claim 29 including: means for identifying a virtual address for sending data from the source node to the destination node and means for providing the virtual address to the source node. (Column 6 Lines 50-55, Column 8 Lines 50-65)

With respect to Claim 37, Iwata discloses the computer system of claim 36 wherein the identified virtual address is not currently used by any source-side ports of switches of the path. (Column 6 Lines 55-65, Column 12 Lines 1-5)

With respect to Claim 38, Iwata discloses the computer system of claim 36 wherein each port of each switch has a virtual address table for mapping virtual addresses to another port of the switch. (Column 10 Lines 30-65)

With respect to Claim 39, Iwata discloses the computer system of claim 29 wherein the path comprises switches with ports and when data is received at a port of a switch, the virtual address of the data is used to retrieve an indication of another port and the data is sent out of the switch through the other port. (Column 10 Lines 30-65, Column 11 Lines 1-35)

With respect to Claim 40, Iwata discloses the computer system of claim 29 wherein the data is a Fibre Channel frame. (Column 1 Lines 1-25) The Examiner notes that the Fibre Channel protocol was designed to operate on ATM networks.

With respect to Claim 41, Iwata discloses the computer system of claim 29 wherein the data is an InfiniBand frame. (Column 1 Lines 1-25) The Examiner notes that the Fibre Channel protocol was designed to operate on ATM networks.

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Conclusion


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please refer to the enclosed PTO-892 form.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Greg Bengzon whose telephone number is (571) 272-3944. The examiner can normally be reached on Mon. thru Fri. 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Cuchlinski can be reached on (571)272-3925. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gcb


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